

REMARKS

Claims 1-63 are pending. Claims 25-63 were withdrawn from consideration. In this paper, claims 1-24 are amended. No new subject matter is added. Reconsideration and allowance of claims 1-24 is respectfully requested in light of the above amendments and following remarks.

Reopen Prosecution

The applicants thank the Examiner for reopening prosecution on this application. However, the applicants still wish to maintain their arguments submitted in the Appeal Brief regarding Kumanoya, Lee, and Luscher references.

Despite the Examiner's characterization of the applicants' discussion regarding the meaning of the phrase "precharge signal" in the Appeal Brief, each statement was taken almost verbatim from the specification. Furthermore, the applicants disagree that they are "totally disregarding" the "broadest reasonable interpretation" (see, e.g., MPEP 2111). At any rate, those rejections are now rendered moot by the newly cited art.

Claim Rejections – 35 USC § 112

Claims 6, 13, and 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, it is allegedly not understandable how the recited "word line precharge signal" relates to the recited "voltage generator" because the claim does not recite a memory circuit.

It is believed that the amendments to claims 1, 7, and 17, upon which claims 6, 13, and 24 depend, respectively, render this rejection moot. In short, claims 1 and 7 now recite, *inter alia*, "a voltage generator configured to bias a word line" and claim 17 now recites, *inter alia*, "a method for biasing a word line." These amendments are explained below in more detail.

Claim Rejections – 35 USC § 103

Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over newly cited art to U.S. Patent No. 5,367,489 issued to Park (hereafter, 'Park') in view of newly cited reference to U.S. Patent No. 5,856,918 issued to Soneda et al. (hereafter, 'Soneda'). The applicants respectfully disagree.

It is alleged that Park FIG. 1B discloses the claimed first charge pump (C5, C6 and the unlabelled transistors connected thereto); the claimed oscillator (OSC); the claimed second charge pump (C1-C4, G1-G4, and unlabelled transistors receiving Φ_{PHB}); and the word line precharge signal (Φ_{PHB}).

The Examiner is asked to direct his attention to the enclosed IDS reference, “A 1-Mbit BiCMOS DRAM Using Temperature Compensation Circuit Techniques”, which is found in the IEEE Journal of Solid-State Circuits, Vol. 24, No. 3, June 1989, disclosed by Kitsukawa et al. (hereafter, “Kitsukawa”).

The upper half of Kitsukawa FIG. 6 is the prior art voltage pumping circuit illustrated by Park FIG. 1B (see Park; column 1, lines 52-56). It is apparent that the alleged first charge pump of Park FIG. 1B (C5, C6, and unlabeled transistors) is not a charge pump at all, but a level compensator (see Kitsukawa FIG. 6 and page 598, section B). In particular, the Vch generator of Kitsukawa FIG. 6 consists of a multistage **pump circuit which is driven by clocks $\Phi 1$, $\Phi 2$, and ΦPH ... synchronized to the level compensator** (page 598, Section B, start of second paragraph; emphasis added).

Thus, since the alleged first charge pump of Park’s FIG. 1B is not actually a charge pump, Park does not disclose a first charge pump and second charge pump with connections as recited in claims 1, 8, and 14. Soneda is not alleged to disclose these features that were attributed to Park.

Consequently, the Park/Soneda combination fails to establish a *prima facie* case of obviousness for claims 1, 8, and 14 because the combination does not teach or suggest all the features recited in those claims (MPEP 2143.03). Claims 2-6 inherently contain the features of claim 1, and claims 15 and 16 inherently contain the features of claim 14. Consequently, the Park/Soneda combination also fails to establish *prima facie* obviousness for claims 2-6 and 15-16 because the combination fails to teach or suggest all the features inherent to those claims (MPEP 2143.03).

Furthermore, claim 1 is amended to recite, *inter alia*, a voltage generator configured to bias a word line from a boosted voltage having a first polarity to a second voltage having a second polarity. This amendment is fully supported by the original disclosure at, e.g., page 2, lines 7-10 and at page 5, lines 1-4.

It is apparent that the pumping circuit illustrated by Park FIG. 1B does not teach or suggest this feature, for the following reasons.

The word line precharge signal alternates between Vpp (standby mode) and ground (operational mode) (FIG. 1B; column 1, lines 60-65). When the word line precharge signal transitions from Vpp to 0V, the signal lines G3 and G4 are pumped to **a level Vpp which is greater than level Vcc** (FIG. 1B; column 1, line 66 to column 2, line 8; emphasis added). When the word line precharge signal transitions from 0V to Vpp, the **signal lines G3 and G4 are returned to level Vcc** (FIG. 1B; column 2, lines 9-18). Park teaches that Vpp and Vcc are

both positive voltages (column 1, lines 66-68). Thus, V_{pp} and V_{cc} are voltages of the same polarity. These statements reflect the teachings of Kitsukawa (see page 598, section B; and also FIGS. 6 and 7).

Consequently, Park FIG. 1B does not teach or suggest the claimed feature of a voltage generator configured to bias a word line from a boosted voltage having a first polarity to a second voltage having a second polarity.

Regarding Soneda, FIGS. 2 and 3 illustrate a booster circuit that produces a boosted voltage of $4V_{cc}$ (see FIG. 4J). FIGS. 8 and 9 illustrate a booster circuit that produces a boosted voltage of $-3V_{cc}$ (see FIG. 10J). The Examiner is apparently using Soneda only to bolster the statement that many environments require a negative [boosted] voltage word line rather than a positive boosted voltage.

However, even if the teaching of Soneda was combined with Park, Soneda FIG. 10J illustrates that the output V_{outB} ranges between ground and $-3V_{cc}$. In other words, Soneda's voltage generator is not configured to bias a word line from a boosted voltage having a first polarity to a second voltage having a second polarity, as recited in claim 1.

In sum, neither Park nor Soneda are directed towards a back biasing scheme for the word lines of non-selected memory cells as taught by the applicant (see, e.g., page 1, lines 15-18; page 2, lines 3-13; page 5, lines 1-4).

For this additional reason, the Park/Soneda combination fails to establish a *prima facie* case of obviousness with respect to claim 1 because the combination fails to teach or suggest the feature recited in the amendment to claim 1 (MPEP 2143.03).

Regarding claims 2-6, they are amended for consistency with claim 1. Since each of the claims inherently contains the features of claim 1, the Park/Soneda combination also fails to establish *prima facie* obviousness for claims 2-6 because it fails to teach or suggest the feature recited in the amendment to claim 1 (MPEP 2143.03).

With regard to claim 7, it is amended in a manner similar to claim 1. The amendment is fully supported by the original disclosure at, e.g., page 2, lines 7-10 and at page 5, lines 1-4. Claims 8-13 are amended for consistency with claim 7, and inherently contain the features of claim 7. Consequently, the Park/Soneda combination also fails to establish a *prima facie* case for claims 7-13 because the combination does not teach the feature recited in the amendment to claim 7 (MPEP 2143.03).

With regard to claim 14, it is amended in a manner similar to claims 1 and 7. The amendment is fully supported by the original disclosure at, e.g., page 2, lines 7-10 and at page 5, lines 1-4. Claims 15-16 are amended for consistency with claim 14, and inherently

contain the features of claim 14. Consequently, the Park/Soneda combination also fails to establish a *prima facie* case for claims 14-16 because the combination does not teach the feature recited in the amendment to claim 14.

With regard to claim 17, it is amended in a manner similar to claims 1, 7, and 14. The amendment is fully supported by the original disclosure at, e.g., page 2, lines 7-10 and at page 5, lines 1-4. Claims 18-24 are amended for consistency with claim 17, and inherently contain the features of claim 17. Consequently, the Park/Soneda combination fails to establish a *prima facie* case for claims 17-24 because the combination does not teach the feature recited in the amendment to claim 17.

Furthermore, the applicants do not believe that the new features recited in amended claims 1, 7, 14, and 17 are taught or suggested by the previously cited Kumanoya, Lee, and Luscher references.

Conclusion

For the foregoing reasons, reconsideration and allowance of claims 1-24 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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Respectfully submitted,

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